CLS-201 CAMERA LINK™ SIMULATOR

User's Manual

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1. Introduction

1.1. Overview

The CLS-201 Camera Link™ [1] simulator is a capable and flexible video test pattern generator supporting Camera Link™ "base" and "medium" configurations. Fully programmable video timing enables the CLS-201 to mimic the characteristics of virtually any base/medium camera.

The CLS-201 is controlled using any PC, workstation, or terminal with a standard RS-232 serial port. CLS-201 control is performed via a simple, straightforward, Command Line Interface (CLI). No special software is required. Template configuration files are provided which can be easily modified with user parameters and downloaded to the CLS-201. CLS-201 default (power-up) configuration is user programmable. This provides convenient recall of saved parameters and enables CLS-201 operation without a host computer.

The CLS-201 Camera Link™ Simulator is extremely useful for the development, test, integration, and field service of Camera Link™ products and systems. Housed in a sturdy aluminum enclosure, the CLS-201 is well suited for industrial environments

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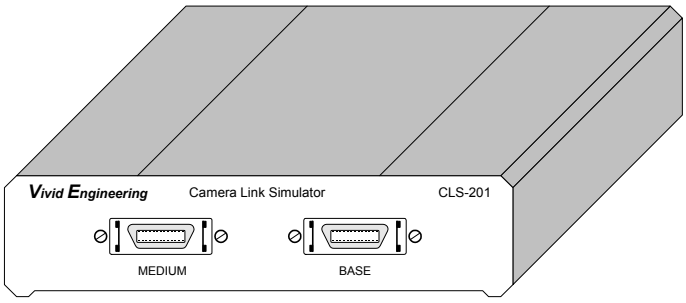
[1] The Camera Link™ interface standard enables the interoperability of cameras and frame grabbers, regardless of vendor. The Automated Imaging Association (AIA) sponsors the Camera Link™ program including the oversight Camera Link Committee, the self-certification program, and the product registry. The Camera Link™ specification may be downloaded from the AIA website, found at www.machinevisiononline.org


Vivid Engineering
Camera Link Simulator
CLS-201
MEDIUM
BASE

1.2. Features

- Capable and flexible video test pattern generator
- Supports Camera Link™ "base" and "medium" configurations
- Fully programmable video timing; mimics virtually any camera
- Area and line scan formats, image sizes to 64Kx64K
- Box, line, horizontal/vertical/diagonal wedge test patterns
- "Roll" feature adds pattern motion
- Triggered (exsync) mode
- Connects to host PC/workstation/terminal serial port (RS-232)
- Controlled via a simple Command Line Interface (CLI)
- Example downloadable configuration files are easily modified w/ user settings
- Requires no special software
- Non-volatile save/recall of user settings
- Can operate stand-alone
- Sturdy, compact aluminum enclosure
- External power supply and RS-232 cable included
- 3-year warrantee

1.3. Functional Description

The CLS-201 Camera Link™ Simulator is a programmable video test pattern generator supporting Camera Link™ "base" and "medium" configurations. A block diagram of the CLS-201 is provided in Figure 1-1. Detailed descriptions of the functional blocks are provided in the following sections.

The CLS-201 combines video test pattern generation circuits implemented in Field Programmable Gate Array (FPGA) technology with an on-board microcontroller. The FPGA-based video test pattern circuitry provides the desired video timing, active window, and test pattern characteristics. The microcontroller links the pattern generation circuitry to the host computer and incorporates a simple, straightforward Command Line Interface (CLI). This enables the CLS-201 to be controlled using any computer incorporating a standard RS-232 serial port. Users may interactively assign settings via the CLI, or may download configuration files created in advance. The CLS-201 incorporates non-volatile memory for storing user configuration settings. Saved settings are automatically loaded upon power-up, enabling operation of the CLS-201 using prestored parameters without a host computer.

The CLS-201 Camera Link™ Simulator incorporates a clock synthesizer which enables the user to select virtually any test pattern clock frequencies within the Camera Link™ 20-66 MHz range. The camera control inputs of the Camera Link™ interface are sent to timing generator for use as exsync inputs, enabling the frame grabber to trigger pattern generation. The serial link in the Camera Link™ interface is looped back to the frame grabber, enabling loopback test of the serial interface.

The CLS-201 camera interface incorporates the connector, signals, pinout, and chipset in compliance with the Camera Link™ specification. The CLS-201 incorporates the "base" and "medium" configuration signal sets, consisting of video data, camera control, and serial communications.

The CLS-201 is powered by an external wall plug-in power supply which is included. Also included is an RS-232 serial cable.

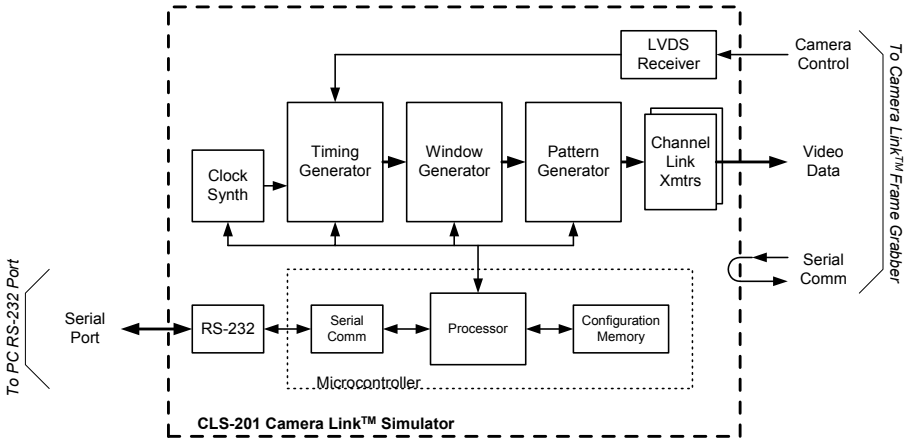


Figure 1-1: CLS-201 Block Diagram

1.3.1. Clock Synthesizer

The CLS-201 Camera Link™ Simulator incorporates a clock synthesizer circuit to generate the reference clock for the video test patterns. The clock synthesizer is capable of generating virtually any reference clock frequency in the Camera Link™ 20-66 MHz range. The reference clock is used by the timing, window, and pattern generation circuitry and is also sent to the frame grabber via the Camera Link™ interface. As with all CLS-201 user parameters, clock frequency settings are stored to non-volatile memory in response to a parameter save command. Stored clock settings are automatically retrieved from memory upon power-up, or in response to a parameter recall command. The CLS-201 clock synthesizer chip is an ICS307M-02 made by Integrated Clock Solutions, Inc. (ICS).

The CLS-201 Command Line Interface (CLI) incorporates two commands for selecting the reference clock frequency. With the *frequency* command, the user simply specifies an integer frequency between 20 and 66 MHz (i.e. 20,21,22…66).

For fractional frequencies (i.e. 27.375 MHz), the *synth_code* command allows direct input of the programming code into the clock synthesizer chip. An online synthesizer code generation tool is available on the Integrated Clock Solutions (ICS) website at http://www.icst.com/products/ics307inputForm.html. Follow the link and enter the following parameters into the window:

- In the Input Frequency box, enter "14.31818"
- Enter desired frequency
- Enter desired accuracy
- In the Clock 2 Output box, select "OFF"
- In the Output Driver box, select "CMOS"
- In the Crystal Load Capacitance box, select "00"
- Click on the "Calculate" button

Example: Running the tool for a desired frequency of 27.375 MHz will return several codes based on best accuracy, lowest jitter, etc. The best accuracy code is 0x348939. To load this code into CLS-201, type "SYNTH_CODE 0x348939" at the command line prompt.

1.3.2. Timing Generator

The CLS-201 Camera Link™ Simulator timing generator establishes the basic video timing characteristics by generating the Line Valid (LVAL) and Frame Valid (FVAL) timing signals. The circuit operates at the reference clock frequency programmed into the clock synthesizer.

LVAL is used to envelope *lines* of video data and is defined in the Camera Link™ specification as *high* for valid line data. Two CLS-201 timing parameters, LVAL_LO and LVAL_HI, determine the duration of LVAL low and high states in pixel clock cycles, respectively. The frequency of the pixel clock is determined by the clock synthesizer. The CLS-201 supports "LVAL low" and "LVAL high" times from 1-65535 pixel clocks. LVAL timing characteristics are shown in Figure 1-2.

Note: The LVAL timing signal is continuously output whenever the CLS-201 is operated in framescan mode. For linescan mode, LVAL is continuous when in operating in "continuous" mode. For linescan mode with exsync triggering, a single LVAL pulse is issued in response to each triggering event.

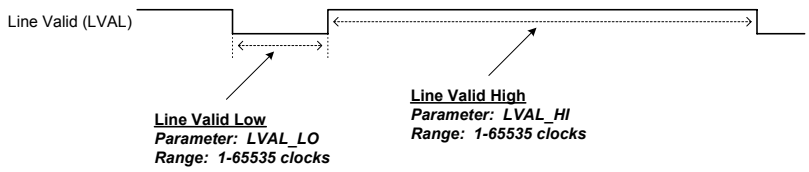


Figure 1-2: Line Valid (LVAL) Timing Characteristics

FVAL is used to envelope *frames* of video data from framescan cameras and is defined in the Camera Link™ specification as *high* for valid frame data. Two CLS-201 timing parameters, FVAL_LO and FVAL_HI, determine the duration of FVAL low and high states in video lines, respectively. Video lines refer to the Line Valid (LVAL) signal which was discussed in the prior paragraph. The CLS-201 supports FVAL low and FVAL high times from 1-65535 lines. FVAL timing characteristics are shown in Figure 1-3.

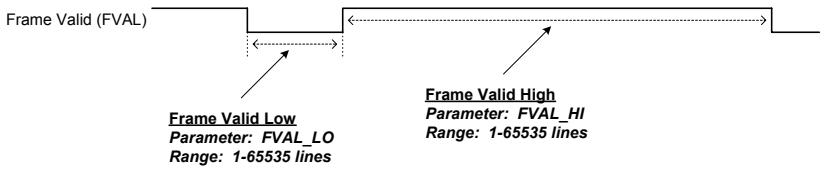


Figure 1-3: Frame Valid (FVAL) Timing Characteristics

The relative positioning of the FVAL and LVAL timing signals is programmable and is specified using the Frame Valid Setup (FVAL_SETUP) and Frame Valid Hold (FVAL_HOLD) parameters.

When FVAL_SETUP and FVAL_HOLD are both set to 0, the default condition occurs whereby transitions on the FVAL signal occur coincident with the falling edge of the LVAL signal (the start of the horizontal blank interval). This relationship is illustrated in Figure 1-4.

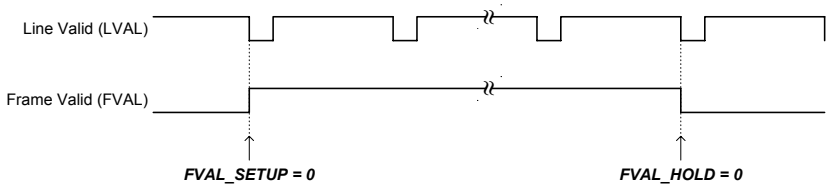


Figure 1-4: Default LVAL/FVAL Timing Relationship

The FVAL_SETUP and FVAL_HOLD parameters allow CLS-201 timing characteristics to be fine tuned in order to mimic camera characteristics, verify frame grabber functionality, etc. Figure 1-5 illustrates how a value inserted in the FVAL_SETUP results in the rising edge of FVAL occurring *in advance of* the falling edge of LVAL. The figure also illustrates how FVAL_HOLD values result in the falling edge of FVAL occurring *after* the falling edge of LVAL.

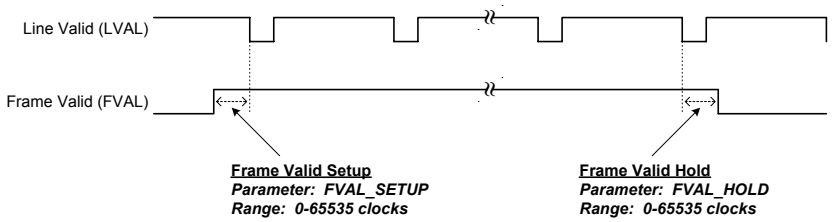


Figure 1-5: FVAL Setup/Hold Timing Parameters

1.3.3. Window Generator

The CLS-201 Camera Link™ Simulator incorporates a programmable window generator that determines the size and position of the video test pattern. The window generator accepts four parameters to determine the position and size of the video test pattern relative to the FVAL and LVAL timing signals described in Section 1.3.2

The starting position of the video test pattern is determined by the X Offset (XOFF) and Y Offset (YOFF) parameters. XOFF determines the staring position within a line ("x" position), and the YOFF parameter determines the starting row ("y" position).

Test pattern image size is defined using the XACT and XOFF parameters. X Active (XACT) determines the horizontal test pattern size in pixels, and Y Active (YACT) determines the vertical pattern size in lines.

Figure 1-6 shows the test pattern line positioning relative to LVAL. Figure 1-7 illustrates the window generation characteristics based on XOFF, YOFF, XACT, and XACT.

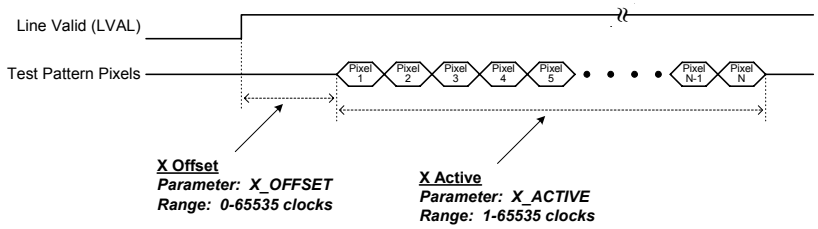


Figure 1-6: Horizontal (X) Offset/Active Parameters

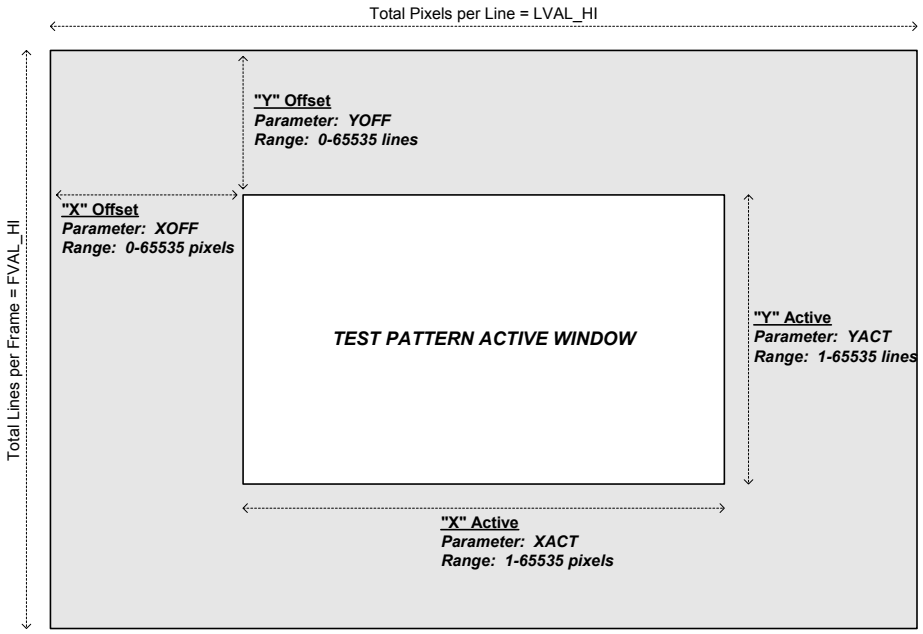


Figure 1-7: Window Generator Characteristics

1.3.4. Pattern Generator

The CLS-201 Camera Link™ Simulator incorporates a programmable pattern generator to create a variety of test patterns. The CLS-201 is capable of generating rectangular fixed-value, horizontal wedge, vertical wedge, and diagonal wedge patterns as shown in Figures 1-8 through 1-11. The rectangular fixed-value pattern may be any width or height (i.e. vertical line, horizontal line, dot, square, etc), in any position, and with selectable foreground and background pixel values.

The CLS-201 enables the user to individually select the test pattern for up-to four pixel outputs (A/B/C/D) in the multi-tap and color modes. To support this feature, four Pattern Select (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL) parameters are provided. The PATSEL parameters are defined in Table 1-1.

Table 1-1: PATSEL Parameter Definition

Pattern Select Value (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL)	Video Test Pattern
0	Fixed Value (rectangular)
1	Horizontal Wedge
2	Vertical Wedge
3	Diagonal Wedge

For the fixed value pattern, four Pixel Fixed Value (A_FIXED, B_FIXED, C_FIXED, D_FIXED) parameters are provided to individually select static pixel values for the up-to four pixels being output.

For the fixed value pattern, the CLS-201 enables the user to individually select the fixed value for each of the up-to four pixel outputs (A/B/C/D). To support this feature, four Pixel Fixed Value (A_FIXED, B_FIXED, C_FIXED, D_FIXED) parameters are provided.

The CLS-201 enables the user to select background pixel values. These are the default output pixel values at all times outside the active video region defined by the window generator. The CLS-201 enables the user to individually select the background value for each of the up-to four pixel outputs (A/B/C/D). To support this feature, four Pixel Background Value (A_BACK, B_BACK, C_BACK, D_BACK) parameters are provided.

The CLS-210 "roll" feature used in conjunction with the wedge patterns (horizontal, vertical, diagonal) to introduce test pattern motion. When roll is enabled, the starting pixel value in the video test pattern increments every frame. This changes all pixel values within the pattern every frame and adds a "rolling" motion to the displayed pattern. This feature is particularly useful during testing and for debugging image acquisition problems.

The CLS-201 supports all modes defined in the Camera Link™ specification for both the "base" and "medium" configurations. These modes range from simple 8-bit single-tap, to 12-bits and 4-taps. The desired mode is selected using the Camera Link Mode (CL_MODE) parameter. The CL_MODE parameter is defined in Table 1-2.

For simplicity ,the CLS-201 refers to A-B-C-D "pixels", not "ports". The CLS-201 outputs up-to four pixels simultaneously, depending on Camera Link™ mode. The pixel values are automatically mapped to their corresponding port assignments as defined in the Camera Link™ specification.

Table 1-1: CL_MODE Parameter Definition

CL_MODE Parameter Setting (decimal)	Camera Link Mode
0	8-bit x 1~3 (base config)
1	10-bit x 1~2 (base config)
2	12-bit x 1~2 (base config)
3	14-bit x 1 (base config)
4	16-bit x 1 (base config)
5	24-bit RGB (base config)
8	8-bit x 4 (medium config)
9	10-bit x 3~4 (medium config)
10	12-bit x 3~4 (medium config)
11	30-bit RGB (medium config)
12	36-bit RGB (medium config)

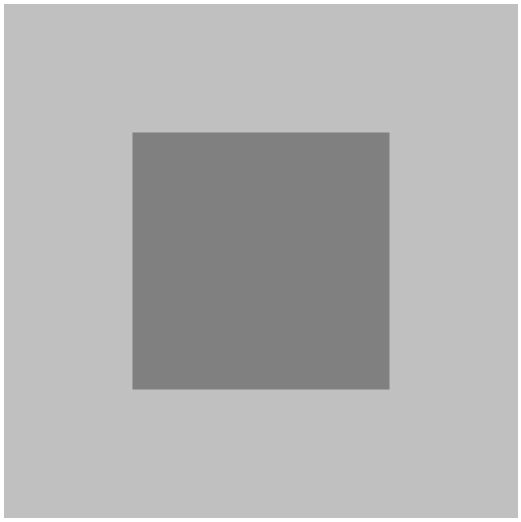


Figure 1-8: Fixed (Rectangular) Test Pattern

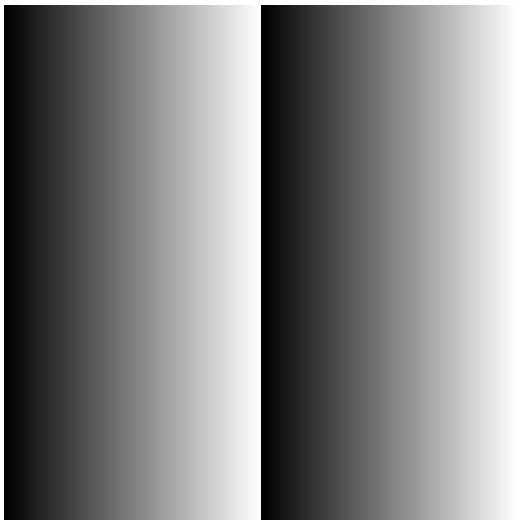


Figure 1-9: Horizontal Wedge Test Pattern

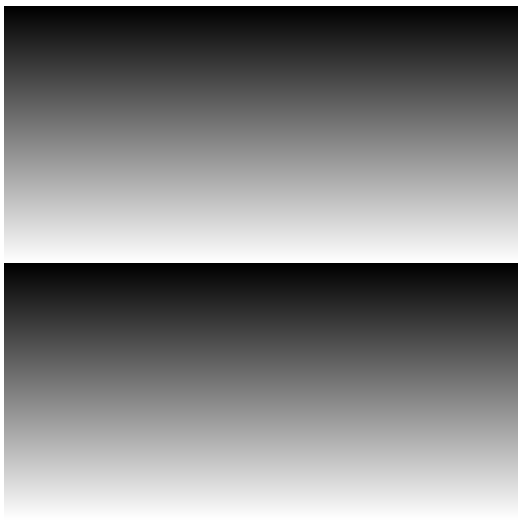


Figure 1-10: Vertical Wedge Test Pattern

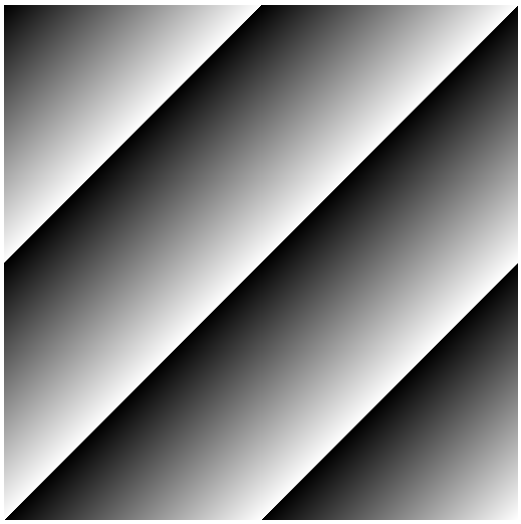


Figure 1-11: Diagonal Wedge Test Pattern

1.3.5. Microcontroller

The CLS-201 Camera Link™ Simulator utilizes a microcontroller device to implement a Command Line Interface (CLI). The CLI enables a PC or workstation to control and monitor CLS-201 functions. The microcontroller interprets commands received over the CLI and configures the CLS-201 circuitry accordingly. The serial communication protocol between the PC/workstation and the CLS-201 is supported by the microcontroller's built-in Universal Asynchronous Receiver/Transmitter (UART).

The microcontroller incorporates non-volatile configuration memory for the storage of user-selected parameters. Upon power-up initialization, the CLS-201 automatically recalls the parameter set stored in memory. This feature enables operation of the CLS-201 without a control port connection. The CLI Parameter Save (SAVE) command is used to store the current parameter set to the configuration memory. The CLI Parameter Recall (RECALL) command configures the CLS-201 using the parameter set currently stored.

1.3.6. RS-232 Serial Port

The CLS-201 Camera Link™ Simulator incorporates an industry-standard RS-232 serial port for linking the CLS-201 to a host PC or workstation. The serial port provides RS-232 signal characteristics and incorporates a standard 9-pin D-Sub (DB9) connector. The serial port protocol settings are conventional and are defined in Table 1-3. Connector information is provided in Section 2.2.

Table 1-3: RS-232 Serial Port Settings

Port Characteristic	Setting
Rate (bits per second)	9600
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None

1.3.7. Camera Control Inputs

The CLS-201 Camera Link™ Simulator receives four Camera Control (CC1, CC2, CC3, CC4) from the frame grabber as defined in the Camera Link™ specification. The camera control signal states can be monitored using the CLI, or used as an exsync input to trigger frame/line output.

CLS-201 can be programmed to select a camera control input (CC1, CC2, CC3, or CC4) for use as an exsync trigger. Exsync trigger polarity (rising or falling edge) is also programmable. When configured, the CLS-201 will issue a single frame (or line in linescan mode) in response to each exsync trigger received.

1.3.8. Channel Link Transmitters

The CLS-201 Camera Link™ Simulator incorporates Channel Link transmitter devices for outputting video timing, data, and clock in compliance with the Camera Link™ specification. Two Channel Link transmitter devices are used, one for the "base" connector and one for the "medium" connector.

The Channel Link transmitter chips are National Semiconductor DS90CR285MTD.

1.4. Command Line Interface (CLI)

The CLS-201 Camera Link™ Simulator incorporates a Command Line Interface (CLI) which enables CLS-201 control and monitoring using virtually any PC, workstation, or terminal. The CLS-201 requires no special software.

Once the CLS-201 is connected to a host computer RS-232 port, the user accesses the CLS-201 using standard communications software. HyperTerminal™ included in the Windows™ software works well as does almost any basic communications software package. By default, the CLS-201 echoes-back all characters received. The Echo Control (ECHO) command enables the user to enable/disable echo. Disabling echo is sometimes desired, in particular when large configuration files are being downloaded to the CLS-201. Serial port settings are listed in Section 1.3.6.

Upon power-up, the CLS-201 initializes for about 2 seconds and then sends the PC a message similar to the following:

```
CLS201 Camera Link Simulator CLI
Vivid Engineering
Rev 1.0
```

The CLS-201 recognizes 38 commands, defined in the following sections. The DUMP, SAVE, and RECALL commands are particularly useful. In the case of invalid syntax, the CLS-201 responds with the following:

```
invalid entry
```

All numeric entries are made using hexadecimal notation only (i.e. 0x20).

CLS-201 parameters may be entered manually on the keyboard, or may be downloaded to the CLS-201 as a configuration file. Configuration files are plain text format (i.e. "*.txt"* files) and may be created with an editor, word processor, etc. Spaces and returns may be inserted as desired for readability. Comments are indicated using a backslash "/" and may be located at the start of a line or following a command. The following is an example of comments located in a configuration file. Note that all numeric information must be in hexadecimal (i.e. 0x20) format. An example configuration file is found in Section 1-5.

```
//   Camera Link Configuration File
//   - syntax example

LVAL_LO     0x0020        // Line Valid Low Setting
LVAL_HI     0x0020        // Line Valid High Setting
```

Methods for downloading text (.txt) files to the CLS-201 vary depending on the communications software used. For HyperTerminal™ (included with Windows™), click on the "Transfer" toolbar and select "Send Text File". HyperTerminal™ will then prompt for the location of the file.

The CLS-201 command set is defined in the following sections.

1.4.1. Line Valid Low (LVAL_LO)

The Line Valid Low (LVAL_LO) command is used to establish the duration, in clock cycles for the "low" (logic 0) portion of the Camera Link™ Line Valid timing signal. See Section 1.3.2 for further information.

Parameter: LVAL_LO
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **LVAL_LO 0xA000**
Read Example: **LVAL_LO ?**

1.4.2. Line Valid High (LVAL_HI)

The Line Valid High (LVAL_HI) command is used to establish the duration, in clock cycles for the "high" (logic 1) portion of the Camera Link™ Line Valid timing signal. See Section 1.3.2 for further information.

Parameter: LVAL_HI
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **LVAL_HI 0xB000**
Read Example: **LVAL_HI ?**

1.4.3. Frame Valid Low (FVAL_LO)

The Frame Valid Low (FVAL_LO) command is used to establish the duration, in lines for the "low" (logic 0) portion of the Camera Link™ Frame Valid timing signal. See Section 1.3.2 for further information.

Parameter: FVAL_LO
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_LO 0xC000**
Read Example: **FVAL_LO ?**

1.4.4. Frame Valid High (FVAL_HI)

The Frame Valid High (FVAL_HI) command is used to establish the duration, in lines for the "high" (logic 1) portion of the Camera Link™ Frame Valid timing signal. See Section 1.3.2 for further information.

Parameter: FVAL_HI
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_HI 0xD000**
Read Example: **FVAL_HI ?**

1.4.5. Frame Valid Setup (FVAL_SETUP)

The Frame Valid Setup (FVAL_SETUP) command determines the number of clock cycles that the rising edge of the Camera Link™ FVAL signal occurs in advance of the falling edge of the LVAL signal. When FVAL_SETUP is set to 0, the rising edge of FVAL is coincident with the falling edge of LVAL. See Section 1.3.2 for further information.

Parameter: FVAL_SETUP
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_SETUP 0xE000**
Read Example: **FVAL_SETUP ?**

1.4.6. Frame Valid Hold (FVAL_HOLD)

The Frame Valid Hold (FVAL_HOLD) command determines the number of clock cycles that the falling edge of the Camera Link™ FVAL signal occurs following the falling edge of the LVAL signal. When FVAL_HOLD is set to 0, the falling edge of FVAL is coincident with the falling edge of LVAL. See Section 1.3.2 for further information.

Parameter: FVAL_HOLD
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_HOLD 0x1000**
Read Example: **FVAL_HOLD ?**

1.4.7. X Offset (X_OFFSET)

The X Offset (X_OFFSET) command determines the number of clock cycles from the rising edge of the Camera Link™ LVAL signal to the start of test pattern data (i.e. horizontal start position). When X_OFFSET is set to 0, line test pattern data begins immediately following the rising edge of LVAL. See Section 1.3.3 for further information.

Parameter: X_OFFSET
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **X_OFFSET 0x2000**
Read Example: **X_OFFSET ?**

1.4.8. X Active (X_ACTIVE)

The X Active (X_ACTIVE) command determines the horizontal size (x dimension) of the test pattern in clock cycles. See Section 1.3.3 for further information.

Parameter: X_ACTIVE
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **X_ACTIVE 0x3000**
Read Example: **X_ACTIVE ?**

1.4.9. Y Offset (Y_OFFSET)

The Y Offset (Y_OFFSET) command determines the number of lines from the rising edge of the Camera Link™ FVAL signal to the start of test pattern data (i.e. vertical start position). When Y_OFFSET is set to 0, the test pattern data begins with the next line. See Section 1.3.3 for further information.

Parameter: Y_OFFSET
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **Y_OFFSET 0x4000**
Read Example: **Y_OFFSET ?**

1.4.10. Y Active (Y_ACTIVE)

The Y Active (Y_ACTIVE) command determines the vertical size (y dimension) of the test pattern in lines. See Section 1.3.3 for further information.

Parameter: Y_ACTIVE
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **Y_ACTIVE 0x5000**
Read Example: **Y_ACTIVE ?**

1.4.11. Pixel "A" Pattern Select (A_PATSEL)

The Pixel "A" Pattern Select (A_PATSEL) command assigns the test pattern for video data pixel "A". The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	A_PATSEL
Settings:	0x0 = Fixed Value
	0x1 = Horizontal Wedge
	0x2 = Vertical Wedge
	0x3 = Diagonal Wedge
Type:	Read/Write

Write Example: **A_PATSEL 0x0**
Read Example: **A_PATSEL ?**

1.4.12. Pixel "B" Pattern Select (B_PATSEL)

The Pixel "B" Pattern Select (B_PATSEL) command assigns the test pattern for video data pixel "B". The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	B_PATSEL
Settings:	0x0 = Fixed Value
	0x1 = Horizontal Wedge
	0x2 = Vertical Wedge
	0x3 = Diagonal Wedge
Type:	Read/Write

Write Example: **B_PATSEL 0x2**
Read Example: **B_PATSEL ?**

1.4.13. Pixel "C" Pattern Select (C_PATSEL)

The Pixel "C" Pattern Select (C_PATSEL) command assigns the test pattern for video data pixel "C". The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_PATSEL
Settings: 0x0 = Fixed Value
0x1 = Horizontal Wedge
0x2 = Vertical Wedge
0x3 = Diagonal Wedge
Type: Read/Write

Write Example: **C_PATSEL 0x2**
Read Example: **C_PATSEL ?**

1.4.14. Pixel "D" Pattern Select (D_PATSEL)

The Pixel "D" Pattern Select (D_PATSEL) command assigns the test pattern for video data pixel "D". The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_PATSEL
Settings: 0x0 = Fixed Value
0x1 = Horizontal Wedge
0x2 = Vertical Wedge
0x3 = Diagonal Wedge
Type: Read/Write

Write Example: **D_PATSEL 0x3**
Read Example: **D_PATSEL ?**

1.4.15. Pixel "A" Fixed Value (A_FIXED)

The Pixel "A" Fixed Value (A_FIXED) command determines the pixel "A" value when the fixed pattern is selected (A_PATSEL = 0). The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_FIXED
Range: Depends on pixel size. 0-65535 *(hex 0x0 - 0xFFFF)* max.
Type: Read/Write

Write Example: **A_FIXED 0xA5A5**
Read Example: **A_FIXED ?**

1.4.16. Pixel "B" Fixed Value (B_FIXED)

The Pixel "B" Fixed Value (B_FIXED) command determines the pixel "B" value when the fixed pattern is selected (B_PATSEL = 0). The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: B_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **B_FIXED 0x5A5**
Read Example: **B_FIXED ?**

1.4.17. Pixel "C" Fixed Value (C_FIXED)

The Pixel "C" Fixed Value (C_FIXED) command determines the pixel "C" value when the fixed pattern is selected (C_PATSEL = 0). The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **C_FIXED 0x3C3**
Read Example: **C_FIXED ?**

1.4.18. Pixel "D" Fixed Value (D_FIXED)

The Pixel "D" Fixed Value (D_FIXED) command determines the pixel "D" value when the fixed pattern is selected (D_PATSEL = 0). The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **D_FIXED 0xC3C**
Read Example: **D_FIXED ?**

1.4.19. Pixel "A" Background Value (A_BACK)

The Pixel "A" Background Value (A_BACK) command determines the default value for video data pixel "A". The default value is output whenever the CLS-201 is not outputting video test pattern data. The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_BACK
Range: Depends on pixel size. 0-65535 *(hex 0x0 - 0xFFFF)* max.
Type: Read/Write

Write Example: **A_BACK 0xA5A5**
Read Example: **A_BACK ?**

1.4.20. Pixel "B" Background Value (B_BACK)

The Pixel "B" Background Value (B_BACK) command determines the default value for video data pixel "B". The default value is output whenever the CLS-201 is not outputting video test pattern data. The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: B_BACK
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **B_BACK 0x5A5**
Read Example: **B_BACK ?**

1.4.21. Pixel "C" Background Value (C_BACK)

The Pixel "C" Background Value (C_BACK) command determines the default value for video data pixel "C". The default value is output whenever the CLS-201 is not outputting video test pattern data. The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_BACK
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **C_BACK 0xC3C**
Read Example: **C_BACK ?**

1.4.22. Pixel "D" Background Value (D_BACK)

The Pixel "D" Background Value (D_BACK) command determines the default value for video data pixel "D". The default value is output whenever the CLS-201 is not outputting video test pattern data. The CLS-201 outputs up-to four pixels simultaneously (A,B,C,D), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_BACK
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **D_BACK 0x3C3**
Read Example: **D_BACK ?**

1.4.23. Camera Link Mode (CL_MODE)

The Camera Link Mode (CL_MODE) command determines the test pattern pixel format. The CLS-201 generates video test patterns for all Camera Link modes supported by the Camera Link™ "base" and "medium" configurations. See Section 1.3.4 for further information.

Parameter:	CL_MODE
Settings:	0x0 = 8-bit x 1~3 (base config)
	0x1 = 10-bit x 1~2 (base config)
	0x2 = 12-bit x 1~2 (base config)
	0x3 = 14-bit x 1 (base config)
	0x4 = 16-bit x 1 (base config)
	0x5 = 24-bit RGB (base config)
	0x8 = 8-bit x 4 (medium config)
	0x9 = 10-bit x 3~4 (medium config)
	0xA = 12-bit x 3~4 (medium config)
	0xB = 30-bit RGB (medium config)
	0xC = 36-bit RGB (medium config)
Type:	Read/Write

Write Example: **CL_MODE 0x2**
Read Example: **CL_MODE ?**

1.4.24. Pattern Roll (ROLL)

The Pattern Roll (ROLL) command adds motion to video test patterns. Roll is used in conjunction with the horizontal, diagonal, or vertical wedge patterns. When ROLL is enabled, the starting pixel value is incremented every frame. This changes all pixel values each frame and adds a "rolling" affect to the video test pattern. When disabled, the wedge test patterns are static (no change from frame to frame). See Section 1.3.4 for further information.

Parameter: ROLL
Settings: 0x0 = Roll disable
0x1 = Roll enabled
Type: Read/Write

Write Example: **ROLL 0x1**
Read Example: **ROLL ?**

1.4.25. Clock Synthesizer Code (SYNTH_CODE)

The Clock Synthesizer Code (SYNTH_CODE) command enables the user to directly enter a 24-bit code into the clock synthesizer device that generates the CLS-201 reference clock. This allows the user to program the reference clock to virtually any frequency in the 20-66 MHz Camera Link™ range. Two commands are provided in the CLS-201 to establish pixel clock frequency; SYNTH_CODE and FREQUENCY. SYNTH_CODE provides maximum flexibility by allowing direct entry of the 24-bit synthesizer code. FREQUENCY provides convenience by allowing the user to select any integer frequency value between 20 and 66. The most –recent SYNTH_CODE or FREQUENCY command determines the frequency. Reads of the clock command not used returns "####". Reads of the clock command used return a value. See Section 1.3.1 for further information.

Parameter: SYNTH_CODE
Settings: 24-bit Synthesizer Device Code
Type: Read/Write

Write Example: **SYNTH_CODE 0x33543D**
Read Example: **SYNTH_CODE ?**

1.4.26. Clock Frequency (FREQUENCY)

The Clock Frequency (FREQUENCY) command enables the user to select integer values for the Camera Link™ reference clock in the 20-66 MHz range. Two commands are provided in the CLS-201 to establish pixel clock frequency; SYNTH_CODE and FREQUENCY. SYNTH_CODE provides maximum flexibility by allowing direct entry of the 24-bit synthesizer code. FREQUENCY provides convenience by allowing the user to select any integer frequency value between 20 and 66. The most –recent SYNTH_CODE or FREQUENCY command determines the frequency. Reads of the clock command not used returns "####". Reads of the clock command used return a value. See Section 1.3.1 for further information.

Parameter: FREQUENCY
Range: 20-66 MHz *(hex 0x14 - 0x42)*
Type: Read/Write

Write Example: **FREQUENCY 0x14**
Read Example: **FREQUENCY ?**

1.4.27. Continuous Mode (CONTINUOUS)

The Continuous Mode (CONTINUOUS) command enables continuous output of video test patterns. When continuous mode is enabled, the CLS-201 outputs continuous video data. When disabled, video pattern data is suspended, awaiting an exsync pulse, one-shot, or return to continuous mode. See Section 1.3.2 for further information.

Parameter: CONTINUOUS
Settings: 0x0 = Continuous Mode Disabled
0x1 = Continuous Mode Enabled
Type: Read/Write

Write Example: **CONTINUOUS 0x1**
Read Example: **CONTINUOUS ?**

1.4.28. Exsync Enable (EXSYNC_ENB)

The Exsync Enable (EXSYNC_ENB) command enables triggered output of pattern frames (or lines in LINESCAN mode) using the camera control inputs (CC1, CC2, CC3, CC4). The exsync camera control input source and active edge are selected using the EXSYNC_SEL command. See Section 1.3.7 for further information.

Parameter: EXSYNC_ENB
Settings: 0x0 = Exsync Triggering Disabled
0x1 = Exsync Triggering Enabled
Type: Read/Write

Write Example: **EXSYNC_ENB 0x1**
Read Example: **EXSYNC_ENB ?**

1.4.29. Exsync Select (EXSYNC_SEL)

The Exsync Select (EXSYNC_SEL) command select which camera control input and active edge is used when generating exsync-triggered video patterns. The CLS-201 supports exsync triggered frame generation using any of Camera Link™ camera control inputs. The triggering edge is selectable as "rising" (low-to-high transition) or "falling" (high-to-low transition). See Section 1.3.7 for further information.

Parameter: EXSYNC_SEL
Settings: 0x0 = CC1 rising edge
0x1 = CC1 falling edge
0x2 = CC2 rising edge
0x3 = CC2 falling edge
0x4 = CC3 rising edge
0x5 = CC3 falling edge
0x6 = CC4 rising edge
0x7 = CC4 falling edge
Type: Read/Write

Write Example: **EXSYNC_SEL 0x7**
Read Example: **EXSYNC_SEL ?**

1.4.30. Linescan Mode (LINESCAN)

The Linescan Mode (LINESCAN) command places the CLS-201 in linescan mode. When linescan mode is disabled, the CLS-201 defaults to framescan mode. See Section 1.3.2 for further information.

Parameter: LINESCAN
Settings: 0x0 = Framescan Mode
0x1 = Linescan Mode
Type: Read/Write

Write Example: **LINESCAN 0x0**
Read Example: **LINESCAN ?**

1.4.31. DVAL State (DVAL)

The DVAL State (DVAL) command determines the static state of the Camera Link™ Data Valid output signal.

Parameter: DVAL
Settings: 0x0 = DVAL output set to 0
0x1 = DVAL output set to 1
Type: Read/Write

Write Example: **DVAL 0x0**
Read Example: **DVAL ?**

1.4.32. CC State (CC)

The CC State (CC) command is used to read the current state of the Camera Link™ camera control inputs (CC1,CC2,CC3,CC4). This register is read only. See Section 1.3.7 for further information.

Parameter: CC
Bit positions: bit 0 = CC1 (lsb)
bit 1 = CC2
bit 2 = CC3
bit 3 = CC4
bit 4-7 = 0
Type: Read

Read Example: **CC ?**

1.4.33. FPGA Version (VERSION)

The FPGA Version (VERSION) command is used to read the hardware version code for the CLS-201 Field Programmable Gate Array (FPGA) device. The standard version code is 0x20.

Parameter: VERSION
Settings: 8-bit FPGA version code (0x20 standard)
Type: Read

Read Example: **VERSION ?**

1.4.34. One Shot Trigger (ONE_SHOT)

The One Shot Trigger (ONE_SHOT) command enables the triggering of a single frame (or line for linescan mode) via the CLI. Note that continuous mode must be disabled to use this feature (see CONTINUOUS command). There is no read or write data associated with this command. See Section 1.3.2 for further information.

Parameter: ONE_SHOT
Settings: None, command only
Type: Command

Example: **ONE_SHOT**

1.4.35. Parameter Save (SAVE)

The Parameter Save (SAVE) command stores the current CLS-201 parameter set to non-volatile memory. The saved parameters are recalled automatically following power-up, or in response to the RECALL command. Saved parameters are maintained until altered via a subsequent SAVE command. There is no read or write data associated with this command. See Section 1.3.5 for further information.

Parameter: SAVE
Settings: None, command only
Type: Command

Example: **SAVE**

1.4.36. Parameter Recall (RECALL)

The Parameter Recall (RECALL) command retrieves the parameter set currently stored in non-volatile memory. The saved parameters are also automatically recalled during power-up initialization. There is no read or write data associated with this command. See Section 1.3.5 for further information.

Parameter: RECALL
Settings: None, command only
Type: Command

Example: **RECALL**

1.4.37. Echo Control (ECHO)

The Echo Control (ECHO) command controls CLS-201 echo-back of characters received via the control interface. Upon CLS-201 power-up, echo is enabled and the CLS-201 will echoes-back all characters received. Turning off echo disables the echo until re-enabled or a subsequent power-up reset. "ECHO ON" and "ECHO OFF" are useful in configuration files to avoid large amounts of returned data during file download. See Section 1.4 for further information.

Parameter: ECHO
Settings: ON = Enable echo (default)
OFF = Disable echo
Type: Write

Write Example: **ECHO ON**

1.4.38. Parameter Dump (DUMP)

The Parameter Dump (DUMP) command causes the CLS-201 to return the entire current parameter set to the host computer. A typical DUMP command response is shown below.

Parameter: DUMP
Settings: None, command only
Type: Command

Example: **DUMP**

CLS-201 Example Response:

```
LVAL_LO     0x0020
LVAL_HI     0x0100
FVAL_LO     0x0002
FVAL_HI     0x0100
FVAL_SETUP  0x0000
FVAL_HOLD   0x0000
X_OFFSET    0x0000
X_ACTIVE    0x0100
Y_OFFSET    0x0000
Y_ACTIVE    0x0100
A_PATSEL    0x03
B_PATSEL    0x00
C_PATSEL    0x00
D_PATSEL    0x00
A_FIXED     0x0000
B_FIXED     0x0000
C_FIXED     0x0000
D_FIXED     0x0000
A_BACK      0x0000
B_BACK      0x0000
C_BACK      0x0000
D_BACK      0x0000
CL_MODE     0x00
ROLL        0x00
SYNTH_CODE  0x######
FREQUENCY   0x14
CONTINUOUS  0x01
EXSYNC_ENB  0x00
EXSYNC_SEL  0x00
LINESCAN    0x00
DVAL        0x00
CC          0x0F
VERSION     0x20
```

1.5. Typical Application

A typical CLS-201 Camera Link™ Simulator application is shown in Figure 1-12. The CLS-201 is being used to simulate a 4-tap, 8-bit, medium configuration, area-scan camera. To support this medium configuration application, two standard Camera Link™ cables are connected between the CLS-201 and the frame grabber. Note that base configuration applications require only one cable. To control the CLS-201, the included serial cable connects the CLS-201 to a standard PC serial port. An example configuration file (cls201_example.txt) with user-selected parameters is shown in Table 1-4.

HyperTerminal™ (included with Windows™) or other communications software program is used to download the configuration file to the CLS-201. PC serial port settings are conventional and are specified in Section 1.3.6 (9600 baud, 8 data bits, no parity, 1 stop bit, no flow control). Using HyperTerminal™, the configuration file is sent to the CLS-201 by selecting the "Transfer" tab and clicking on "Send Text File". The user then specifies the location of "cls201_example.txt" and file download commences. Alternately, the parameters may be individually entered via the CLI. Subsequent changes to CLS-201 parameters can be made by downloading a new configuration file, or by manually entering commands with the keyboard.

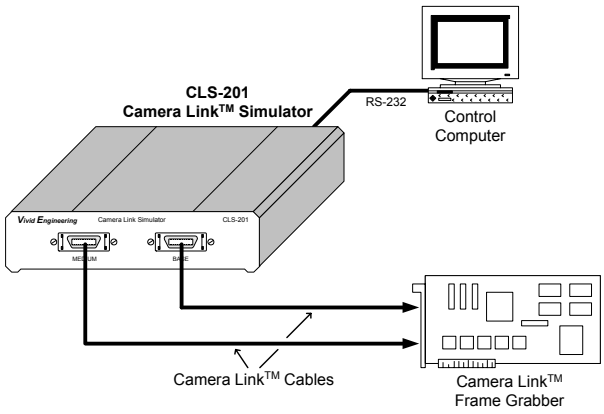


Figure 1-12: CLS-201 Typical Application

Table 1-4: Example Configuration File (cls201_example.txt)

```
//   - Camera Link "medium" configuration
//   - Four 8-bit pixels (4x8)
//   - 512x512 active image area
//   - 20 MHz pixel clock rate
//   - Continuous output mode
//   - Diagonal wedge pattern on all pixels

// Line Valid Low
//   - 32 clocks
LVAL_LO     0x0020        // i.e. decimal 32 = hex 0x20

// Line Valid High
//   - 576 clocks
LVAL_HI     0x0240

// Frame Valid Low
//   - 2 lines
FVAL_LO     0x0002

// Frame Valid High
//   - 512 lines
FVAL_HI     0x0200

// Frame Valid Setup
//   - 0 clocks
FVAL_SETUP  0x0000

// Frame Valid Hold
//   - 0 clocks
FVAL_HOLD  0x0000

// X Offset
//   - 8 clocks
X_OFFSET    0x0008

// X Active
//   - 512 clocks
X_ACTIVE    0x0200

// Y Offset
//   - 0 lines
Y_OFFSET    0x0000

// Y Active
//   - 512 lines
Y_ACTIVE    0x0200
```

```
// Pixel A-B-C-D Pattern Select
//   - a-d = diagonal wedge = 0x3
A_PATSEL    0x03
B_PATSEL    0x03
C_PATSEL    0x03
D_PATSEL    0x03

// Pixel A-B-C-D Fixed Value
//   - a-d = 0x00
A_FIXED     0x00
B_FIXED     0x00
C_FIXED     0x00
D_FIXED     0x00

// Pixel A-B-C-D Background Value
//   - a-d = 0x00
A_BACK      0x00
B_BACK      0x00
C_BACK      0x00
D_BACK      0x00

// Camera Link Mode
//   - mode = medium 8x4 = 0x08
CL_MODE     0x08

// Pattern Roll
//   - roll disabled = 0x00
ROLL        0x00

// Clock Frequency
//   - 20 MHz = 0x14
FREQUENCY   0x14

// Continuous Mode
//   - continuous mode enabled = 0x01
CONTINUOUS  0x01

// Exsync Enable
//   - exsync triggering disabled = 0x00
EXSYNC_ENB  0x00

// Exsync Select
//   - CC1 rising edge = 0x00
EXSYNC_SEL  0x00

// Linescan Mode
//   - linescan mode disabled = framescan mode = 0x00
LINESCAN    0x00

// DVAL State
//   - dval signal state = 1
DVAL        0x01
```

1.6. Specifications

Table 1-5: CLS-201 Specifications

Feature	Specification
Camera Interface	Camera Link™ Spec "base" & "medium" configurations
Camera Connectors	26-pin MDR type (2)
Frequency Range	20 - 66 MHz
Serial Port Interface	RS-232
Serial Port Connector	Male 9-pin D-Sub (DB9)
Serial Port Cable	3 meter DB9 female - DB9 female null modem cable
Chipset	National Semi. DS90CR285 (2)
Power Supply	External 6 VDC Wall Transformer
Power Jack	2.1 x 5.5 mm, center-positive
Power Requirements	210 mA at 6 VDC (typical)
Cabinet Dimensions	5.28" (L) x 1.12" (H) x 6.13" (D)
Weight	14 oz
Operating Temperature Range	0 to 50° C
Storage Temperature Range	-25 to 75° C
Relative Humidity	0 to 90%, non-condensing

2. Interface

2.1. Front Panel Connections

The CLS-201 Camera Link™ Simulator front panel is shown in Figure 2-1. The front panel contains two video connectors for connecting to the frame grabber. Camera Link™ "medium" configurations utilize both video connectors. "Base" configurations utilize only the "base" connector.

The camera connectors are 26-pin MDR type (MDR-26), 3M p/n 10226-55G3VC as specified in the Camera Link™ Specification. Figure 2-2 identifies the MDR-26 pin positions.

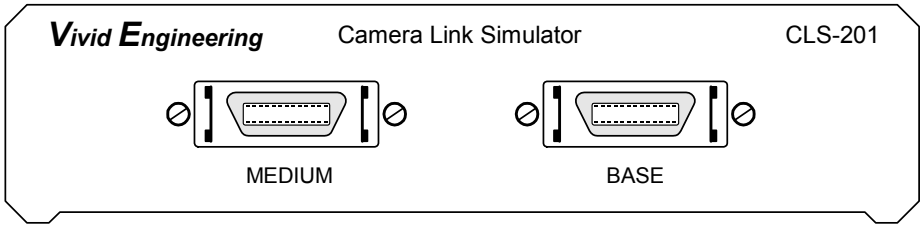


Figure 2-1: CLS-201 Front Panel

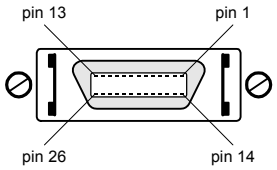


Figure 2-2: MDR-26 Connector Pin Positions

2.1.1. Camera Connector Signals

The MDR-26 camera connector signal assignments are compliant with the Camera Link™ Specification for the "base" and "medium" configurations.

Table 2-1 and 2-2 identify the signal assignments for the MDR-26 "base" and "medium" camera connectors, respectively.

Note that the connector pin assignments are as defined for the camera interface in the Camera Link™ Specification. This provides compatibility with standard Camera Link™ cables

2.1.2. Cable Shield Grounding

Camera Link™ cable "outer" shields are connected to the CLS-201 aluminum case. Case and endplate contacting surfaces are unpainted, providing a Faraday cage to shield internal circuitry. The case is isolated from the CLS-201 circuitry and the cable "inner" shields, avoiding possible safety concerns.

The camera cable "inner" shield connects to circuit digital ground, maintaining signal reference levels between the CLS-201 and the frame grabber.

Table 2-1: CLS-201 "Base" Connector

Camera Link™ Signal Name	"Base" Connector Pin # (camera pinout)	Signal Direction	Notes
Inner shield	1	N/A	*tied to digital ground*
Inner shield	14	N/A	*tied to digital ground*
X0-	2	CLS-201 → FG	
X0+	15	CLS-201 → FG	
X1-	3	CLS-201 → FG	
X1+	16	CLS-201 → FG	
X2-	4	CLS-201 → FG	
X2+	17	CLS-201 → FG	
Xclk-	5	CLS-201 → FG	
Xclk+	18	CLS-201 → FG	
X3-	6	CLS-201 → FG	
X3+	19	CLS-201 → FG	
SerTC+	7	FG → CLS-201	*serial comm*
SerTC-	20	FG → CLS-201	*"*
SerTFG-	8	CLS-201 → FG	*serial comm*
SerTFG+	21	CLS-201 → FG	*"*
CC1-	9	FG → CLS-201	
CC1+	22	FG → CLS-201	
CC2+	10	FG → CLS-201	
CC2-	23	FG → CLS-201	
CC3-	11	FG → CLS-201	
CC3+	24	FG → CLS-201	
CC4+	12	FG → CLS-201	
CC4-	25	FG → CLS-201	
Inner shield	13	N/A	*tied to digital ground*
Inner shield	26	N/A	*tied to digital ground*

"FG" = Frame Grabber

Table 2-2: CLS-201 "Medium" Connector

Camera Link™ Signal Name	"Medium" Connector Pin # (camera pinout)	Signal Direction	Notes
Inner shield	1	N/A	*tied to digital ground*
Inner shield	14	N/A	*tied to digital ground*
Y0-	2	CLS-201 → FG	
Y0+	15	CLS-201 → FG	
Y1-	3	CLS-201 → FG	
Y1+	16	CLS-201 → FG	
Y2-	4	CLS-201 → FG	
Y2+	17	CLS-201 → FG	
Yclk-	5	CLS-201 → FG	
Yclk+	18	CLS-201 → FG	
Y3-	6	CLS-201 → FG	
Y3+	19	CLS-201 → FG	
100 ohm	7	N/A	*100 ohm termination, 7-20*
terminated	20	N/A	*100 ohm termination, 7-20*
	8	N/A	*unused*
	21	N/A	"
	9	N/A	"
	22	N/A	"
	10	N/A	"
	23	N/A	"
	11	N/A	"
	24	N/A	"
	12	N/A	"
	25	N/A	"
Inner shield	13	N/A	*tied to digital ground*
Inner shield	26	N/A	*tied to digital ground*

"FG" = Frame Grabber

2.2. Rear Panel

The CLS-201 Camera Link™ Simulator rear panel is shown in Figure 2-3. The rear panel contains an RS-232 connector, power on indicator, on-off switch, and DC power jack. The DC power jack accepts 6 volts DC, center-positive.

The RS-232 serial port connector is a standard 9-pin male D-Sub type (DB9), Tyco p/n 747840-4. Figure 2-4 identifies the DB9 pin positions.

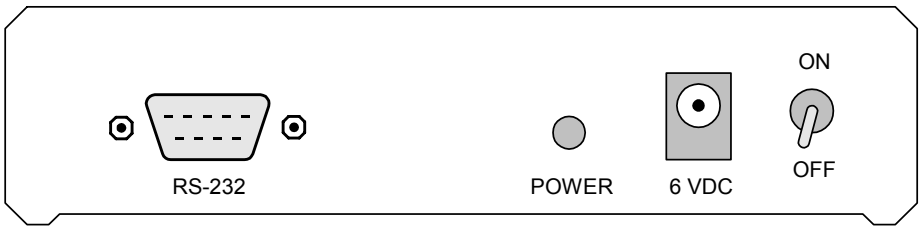


Figure 2-3: CLS-201 Rear Panel

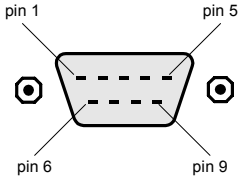


Figure 2-4: DB9 Connector Pin Positions

2.2.1. DB9 Connector Signals

The DB9 connector signal assignments are compliant with the RS-232 serial interface standard. Table 2-3 identifies the DB9 signal assignments.

Table 2-3: DB9 Connector

RS-232 Signal Name	DB9 Pin#	Signal Direction	Notes
Received Line Signal Detect	1	N/A	*unused*
Received Data	2	PC → CLS-201	
Transmitted Data	3	CLS-201 → PC	
Data Terminal Ready	4	N/A	*unused*
Signal Ground (common)	5	N/A	*tied to digital ground*
DCE Ready	6	N/A	*unused*
Request To Send	7	N/A	"
Clear To Send	8	N/A	"
Ring Indicator	9	N/A	"

"PC" = Control PC, workstation, or terminal

3. Mechanical

3.1. Dimensions

The CLS-201 Camera Link™ Simulator cabinet dimensions are shown in Figure 3-1. Note that the dimensions are for the cabinet only. Connectors, switch, hardware, etc are not included in the measurements.

The CLS-201 is housed in a sturdy aluminum enclosure. The body is extruded aluminum, with detachable front and rear endplates.

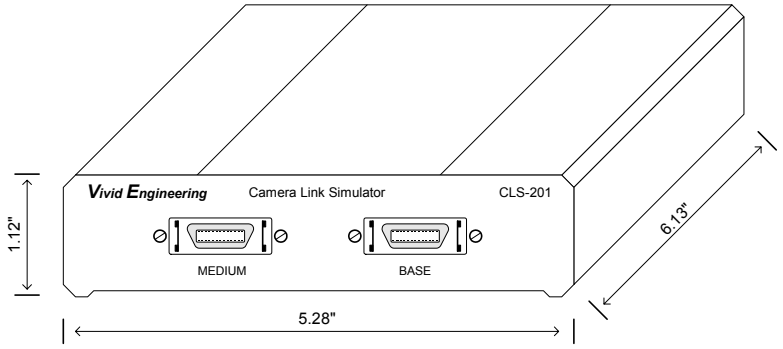


Figure 3-1: CLS-201 Cabinet Dimensions

3.2. External Power Supply

The CLS-201 is powered by an external wall-mount 6 VDC power supply (included). The power supply incorporates a standard 2.1 x 5.5 mm DC power plug. Power plug polarity is center-positive. The power supply is UL and CSA listed.

An EMI filter is located on the power cord near the DC power plug. The filter suppresses EMI emissions.

The CLS-201 is protected by an internal resettable fuse.

4. Revision History

Table 5-1: CLS-201 User's Manual Revision History

Document ID #	Date	Changes
200036-1.1	6/25/03	Initial release of manual
200036-1.2	10/20/03	Adds online clock synthesizer tool info