ADDITIONAL CLS-211 / CLS-212 CONTROL REGISTERS FOR AIA VALIDATION TEST SUPPORT

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The Vivid Engineering model CLS-211 and CLS-212 Camera Link Simulators now incorporate the AIA validation test pattern. The validation test pattern is a 410-frame LFSR (i.e. pseudo-random) sequence used to evaluate the performance of Camera Link components.

Vivid Engineering added a "freeze" mode where only the first LFSR frame of the 410-frame sequence is continuously output. The single frame output is easier to acquire and is useful for general performance testing. In addition, a clock disable feature was added which allows the channel link transmitter chips in the CLS-211/212 to be individually disabled.

The test pattern was introduced in the CLS-211 starting at serial number M17001. CLS-212 starting serial number is B17001.

Several new control resisters have been added to the CLS-211/212 to support the added features. These control register are defined in the following sections.

1.1 AIA Test Pattern (AIA_TEST)

The AIA Test Pattern (AIA_TEST) command enables the 410-frame LFSR test patterns proposed at the Camera Link Committee for FPGA validation purposes. Four test patterns exist, one for each camera Link configuration (80-bit, base, medium, full). Pattern selection is made using the AIA_SEL command described below. When enabled, the CLS-211 / CLS-212 will output the 410-frame pattern in continuous, triggered, or one shot fashion and at the user selected pixel clock frequency as determined by the following control registers:

```
SYNTH_CODE
FREQUENCY
CONTINUOUS
EXSYNC_ENB
EXSYNC_SEL
ONE_SHOT
AIA_SEL
CLK_DIS
```

A "freeze" mode is also provided in which *only* the 1st frame of the 410-frame pattern is output. This single-frame pattern is much easier to acquire and is useful for general functional and performance testing.

Note that the settings in all other control registers are ignored when AIA_TEST = 1 or 3. When AIA_TEST = 0, the CLS-211 / CLS-212 operates as the standard product.

Parameter: AIA_TEST
Settings: 0 (0x0) = AIA test pattern disabled
1 (0x1) = AIA test pattern enabled (410-frame sequence)
3 (0x3) = AIA test pattern enabled (freeze mode, frame 1 of sequence only)
Type: Read/Write

Write Example: **AIA_TEST 1**
Read Example: **AIA_TEST ?**

1.2 AIA Pattern Select (AIA_SEL)

The AIA Pattern Select (AIA_SEL) command selects which Camera Link configuration (base, medium, full, 80-bit) test pattern is issued when the AIA LFSR validation pattern is being generated (i.e. AIA_TEST = 1). Test patterns for base, medium, and full configurations have been added to the original 80-bit pattern at the request of the Camera Link Committee.

Note that when "medium" configuration is selected, it is suggested to set the CLK_DIS register to "1". This will disable the "full" transmitter in the Camera Link interface since there is no full transmitter in a medium configuration interface.

Parameter: AIA_SEL
Settings: 0 (0x0) = 80-bit LFSR pattern

1 (0x1) = Base configuration LFSR pattern
2 (0x2) = Medium configuration LFSR pattern
3 (0x3) = Full configuration LFSR pattern

Type: Read/Write

Write Example: **AIA_SEL 0x1**
Read Example: **EXSYNC_SEL ?**

1.3 Clock Disable (CLK_DIS)

The Clock Disable (CLK_DIS) command provides individual disable control for the clock output signals generated by the Channel Link transmitter chips (i.e. base, medium, full) in the Camera Link interface. When disabled, all associated Camera Link interface signals (i.e. clock + data) are inactive.

Parameter: CLK_DIS
Bit positions: bit 0 = Base transmitter clock output disabled when "1"
bit 1 = Medium transmitter clock output disabled when "1"
bit 2 = Full transmitter clock output disabled when "1"
bit 3-7 = 0
Type: Read/Write

Write Example: **CLK_DIS 0x7**
Read Example: **CLK_DIS ?**

1.4 Example

The following example will continuously output the 410-frame pattern with an 85MHz pixel clock rate over an 80-bit interface:

```
CONTINUOUS  1
FREQUENCY   85
AIA_TEST    1
AIA_SEL     0
CLK_DIS     0
```